REMARKS/ARGUMENTS

Claims 18-34 are pending in this application. By this amendment, Applicant amends Claims 18, 25, and 32.

The Abstract of the Disclosure was objected to because it allegedly exceeds 150 words. Applicant respectfully disagrees. The Abstract of the Disclosure was amended in the Preliminary Amendment filed on September 27, 2006 so as to include 139 words. It appears that the Examiner may have referred to the originally filed Abstract of the Disclosure, which exceeded 150 words, instead of the Abstract of the Disclosure as amended in the Preliminary Amendment filed on September 27, 2006. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this objection.

Claims 18-22, 25-29, 32, and 33 were rejected under 35 U.S.C. § 102(b) as being anticipated by Okura et al. (JP 2000-012377). Claims 23, 24, 30, 31, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Okura et al. in view of Kitamura (U.S. 2002/0093415). Applicant respectfully traverses the rejections of Claims 19, 20, and 22-34.

Claim 18 has been amended to recite:

> A method for manufacturing electronic components, in which conductive pattern layers are laminated to each other with insulating layers provided therebetween to form an integrated laminate, the method comprising the steps of:
>
> alternately laminating the insulating layers and conductive pattern layers including conductive patterns which are formed at intervals therebetween in layer surface directions to form a laminate in which laminate portions of electronic component-forming conductive patterns are collectively formed;
>
> applying a force to the laminate in a lamination direction to form an integrated laminate;
>
> after the force is applied to the laminate in the lamination direction to form the integrated laminate, cutting the laminate along cutting lines provided along boundaries of the laminate portions of the electronic component-forming conductive patterns so as to separate electronic components from each other;

forming at least one removal dummy pattern in at least one of the conductive pattern layers which are to be laminated to each other before one of the insulating layers is provided on a surface of said at least one of the conductive pattern layers, the at least one removal dummy pattern having a size that allows it to be disposed within a cutting-removal region which is a region to be cut and removed by the step of cutting the laminate;

forming at least one floating dummy pattern in at least one of the conductive pattern layers of the laminate portions of the electronic component-forming conductive patterns so as to be disposed in the vicinity of an outside of the cutting-removal region at an interval therefrom before one of the insulating layers is formed by lamination on a surface of said at least one conductive pattern layer, the at least one floating dummy pattern not being electrically connected to the electronic component-forming conductive patterns; and

the at least one removal dummy pattern is not exposed at end surfaces of the separated electronic components. (emphasis added)

Applicant's Claim 25 has been amended to recite:

A mother substrate for forming many electronic components, comprising:

conductive pattern layers having conductive patterns which are formed at intervals therebetween in layer surface directions; and

insulating layers which are alternately arranged with the conductive pattern layers to form a laminate in which laminate portions of electronic component-forming conductive patterns are collectively provided, the laminate being arranged to be cut along cutting lines provided along boundaries of the laminate portions of the electronic component-forming conductive patterns so as to separate the electronic components from each other; wherein

in at least one of the conductive pattern layers, **at least one removal dummy pattern is provided and has a size that allows it to be entirely disposed within a cutting-removal region which is to be cut away along the cutting lines**;

in at least one conductive pattern layers of the laminate portions of the electronic component-forming conductive patterns, at least one floating dummy pattern which is not electrically connected to the electronic component-forming conductive patterns is provided in the vicinity of the outside of the cutting-removal region at an interval therefrom; and

the at least one removal dummy pattern is spaced apart from the cutting lines.

Applicant's Claim 32 has been amended to recite:

> An electronic component comprising:
> conductive pattern layers; and
> insulating layers which are alternately arranged with the conductive pattern layers to form a laminate in which the conductive pattern layers are integrally laminated to each other; wherein
> in at least one of the conductive pattern layers, at least one floating dummy pattern which is not electrically connected to a corresponding conductive pattern is disposed in a region between an end surface of said at least one of the conductive pattern layers and the conductive pattern at an interval therefrom so as not to be exposed at the end surface of said at least one of the conductive pattern layers; and
> **no conductive patterns are disposed between the end surface of said at least one of the conductive pattern layers and the at least one floating dummy pattern**. (emphasis added)

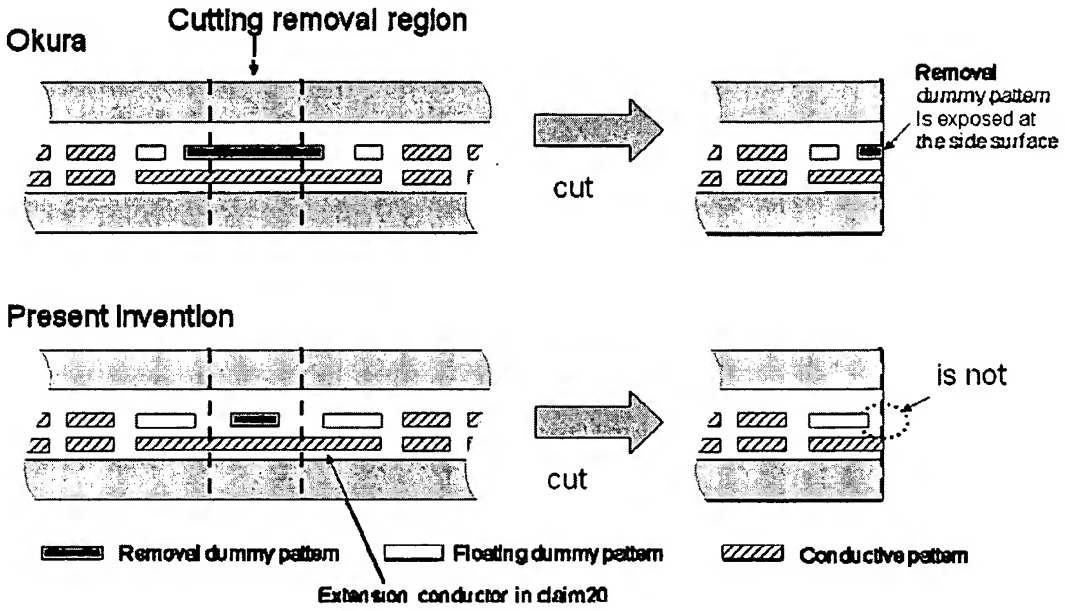
With the unique combination and arrangement of features recited in Applicant's Claims 18, 25, and 32, including the features of "the at least one removal dummy pattern is not exposed at end surfaces of the separated electronic components," "at least one removal dummy pattern is provided and has a size that allows it to be entirely disposed within a cutting-removal region which is to be cut away along the cutting lines," "the at least one removal dummy pattern is spaced apart from the cutting lines," and "no conductive patterns are disposed between the end surface of said at least one of the conductive pattern layers and the at least one floating dummy pattern," Applicant has been able to provide a method of manufacturing electronic components that prevents disadvantageous and unnecessary plating being performed on the removal and floating dummy patterns, and migration between the removal and floating dummy patterns and the conductive pattern (see, for example, paragraphs [0008] and [0015] of the Substitute Specification).

The Examiner alleged that Okura et al. teaches all of the features recited in Applicant's Claims 18, 25, and 32.

Applicant's Claim 18 has been amended to recite the feature of "the at least one

removal dummy pattern is not exposed at end surfaces of the separated electronic components." Applicant's Claim 25 has been amended to recite the features of "at least one removal dummy pattern is provided and has a size that allows it to be entirely disposed within a cutting-removal region which is to be cut away along the cutting lines" and "the at least one removal dummy pattern is spaced apart from the cutting lines." Applicant's Claim 32 has been amended to recite the feature of "no conductive patterns are disposed between the end surface of said at least one of the conductive pattern layers and the at least one floating dummy pattern." Support for these features is found, for example, in paragraphs [0051] to [0054] of the Substitute Specification, and Fig. 3A to Fig. 4 of the originally filed drawings.

As shown in the figures provided below and in Fig. 4 of Okura et al., Okura et al. teaches a straw-man electrode 10, which the Examiner alleged corresponds to the removal dummy pattern recited in Applicant's Claims 18 and 25, that is exposed at an end surface of the separated electronic component. Okura et al. fails to teach or suggest any conductive pattern that is disposed in a cutting removal region and is not exposed at an end surface of the separate electronic component. Furthermore, the straw-man electrode 10 of Okura et al. is only partially disposed in cutting removal region between cutting lines Z and extends across each of the cutting lines Z. Okura et al. fails to teach or suggest any conductive pattern that is entirely disposed in a cutting-removal region.



Thus, Okura et al. certainly fails to teach or suggest the feature of "the at least one removal dummy pattern is not exposed at end surfaces of the separated electronic components" as recited in Applicant's Claim 18, and the features of "at least one removal dummy pattern is provided and has a size that allows it to be entirely disposed within a cutting-removal region which is to be cut away along the cutting lines" and "the at least one removal dummy pattern is spaced apart from the cutting lines" as recited in Applicant's Claim 25.

In addition, as shown in Figs. 5(a) to 6 of Okura et al., each of the conductive patterns 6, 22b, 32a that is not exposed at an end surface of the conductive pattern layers are arranged such that another conductive pattern layer 10, 22a, 32b is disposed between the end surface and the conductive patterns 6, 22b, and 32a. Okura et al. fails to teach or suggest any conductive pattern that is not exposed at an end surface of the conductive pattern layers that is arranged such that no conductive patterns are disposed between the end surface and the at least one floating dummy pattern.

Thus, Okura et al. certainly fails to teach or suggest the feature of "no conductive patterns are disposed between the end surface of said at least one of the conductive

pattern layers and the at least one floating dummy pattern" as recited in Applicant's Claim 32.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 18, 25, and 32 under 35 U.S.C. § 102(b) as being anticipated by Okura et al.

The Examiner relied upon Kitamura to allegedly cure deficiencies of Okura et al. However, Kitamura fails to teach or suggest the feature of "the at least one removal dummy pattern is not exposed at end surfaces of the separated electronic components" as recited in Applicant's Claim 18, and similarly in Applicant's Claim 25, and the feature of "no conductive patterns are disposed between the end surface of said at least one of the conductive pattern layers and the at least one floating dummy pattern" as recited in Applicant's Claim 32. Thus, Kitamura clearly fails to cure the deficiencies of Okura et al. described above.

In view of the foregoing amendments and remarks, Applicant respectfully submits that Claims 18, 25, and 32 are allowable. Claims 19-24, 26-31, 33, and 34 depend upon Claims 18, 25, and 32, and are therefore allowable for at least the reasons that Claims 18, 25, and 32 are allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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